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10/750,714	12/31/2003	Ricardo E. Gonzalez	PA2683US	1388

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EXAMINER	
GEIB, BENJAMIN P	
ART UNIT	**PAPER NUMBER**
2181	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/750,714	GONZALEZ ET AL.	
	Examiner	Art Unit	
	Benjamin P. Geib	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-14,16,18,20-26 and 31-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-14,16,18,20-26 and 31-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received that placed of record in the file: amendment received on 11/07/2007.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 4-6, 8-14, 16, 18, 20-26, and 31-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Borkar et al., "iWarp: An Integrated Solution to High-Speed Parallel Computing" (Hereinafter Borkar) in view of Barat et al., "Reconfigurable Instruction Set Processors: A Survey" (Hereinafter Barat).

4. Referring to claim 1, Borkar has taught a system for processing applications, the system comprising:

a plurality of processor nodes *[iWarp cells; Fig. 1]* with each processor node comprising:

a processing element *[computation agent; Fig. 1]* configured to execute at least one of the applications *[section 2.1]*,

a first communication interface *[first input port/output port pair]* including a first array interface module configured to interface to a first other member of the plurality of processor nodes *[The communication agent of each iWarp cell has 4 input ports and 4 output ports configured to interface to other iWarp cells; section 2.1]*,

a first standard input/output interface *[first input port/output port pair]* configured to communicate with a first input/output device *[The communication agent of each iWarp cell has 4 input ports and 4 output ports configured to interface to other iWarp cells; section 2.1]*,

a second communication interface *[second input port/output pair]* including a second array interface module configured to interface to a second other member of the plurality of processor nodes *[The communication agent of each iWarp cell has 4 input ports and 4 output ports configured to interface to other iWarp cells; section 2.1]*,

a second standard input/output interface *[second input port/output pair]* configured to communicate with a second input/output device *[The communication agent of each iWarp cell has 4 input ports and 4 output ports configured to interface to other iWarp cells; section 2.1]*; and

a plurality of links interconnecting the plurality of processor nodes *[buses; section 2.2]*.

Borkar has not taught that the plurality of processor nodes additionally comprise a software extensible device configured to provide additional new instructions to a set of standard instructions for the processing element wherein the new instructions can be programmed by software.

Barat has taught coupling a reconfigurable processing unit (RPU) to a microprocessor to provide additional new instructions to a set of standard instructions for the microprocessor wherein the new instructions can be programmed by software *[section 1, "Introduction"]*.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the iWarp cells of Borkar to each comprise a software extensible device (i.e. an RPU) coupled to the computation unit of each iWarp cell thereby providing additional new instructions to a set of standard instruction for the computation unit wherein the new instruction can be programmed by software as taught by Barat.

The suggestion/motivation for doing so would have been that processing is more specialized thereby accelerating execution and increasing performance *[section 1, "Introduction"]*.

5. Referring to claim 2, Borkar and Barat have taught the system of claim 1 wherein each one of the processor nodes are on separate chips *[Borkar; 1st paragraph of introduction]*.

6. Referring to claim 4, Borkar and Barat have taught the system of claim 1 wherein two or more of the plurality of the processor nodes are configured in an array *[Borkar; section 3]*.

7. Referring to claim 5, Borkar and Barat have taught the system of claim 1wherein the software extensible device comprises an instruction set extension fabric *[Barat; Since the RPU extends the instruction set, it is an instruction set extension fabric]*.

8. Referring to claim 6, Borkar and Barat have taught the system of claim 1 wherein the software extensible device comprises a programmable logic device *[Barat; section 3.3]*.

9. Referring to claims 8 and 20, taking claim 8 as exemplary, Borkar and Barat have taught the system of claim 1 wherein at least one of the first communication interface and the second communication interface is configured to communicate using message passing *[Borkar; 1st paragraph of section 4.1.1]*.

10. Referring to claims 9 and 21, taking claim 9 as exemplary, Borkar and Barat have taught the system of claim 1 wherein at least one of the first communication interface and the second communication interface is configured to communicate using channels between the processor nodes *[Borkar; 6th paragraph of section 4.1.1]*.

11. Referring to claims 10 and 22, taking claim 10 as exemplary, Borkar and Barat have taught the system of claim 9 wherein at least one of the first communication interface and the second communication interface is configured to perform time division multiplexing using the channels between the processor nodes *[Borkar; 6th paragraph of section 4.1.1]*.

12. Referring to claims 11 and 23, taking claim 11 as exemplary, Borkar and Barat have taught the system of claim 9 wherein at least one of the first communication interface and the second communication interface is configured to perform spatial division multiplexing using the channels between the processor nodes *[Borkar; 6th paragraph of section 4.1.1]*.

13. Referring to claim 12, Borkar and Barat have taught the system of claim 1 wherein at least one of the first communication interface and the second communication interface comprises a processor network interface *[Borkar; the communication interfaces interface a network of processor; section 3]*.

14. Referring to claim 13, Borkar and Barat have taught the system of claim 1 wherein at least one of the first communication interface and the second communication interface comprises a processor network

switch *[Borkar; the communication interfaces switch communications in a network of processors; section 3]*.

15. Referring to claim 14, Borkar and Barat have taught the system of claim 1 wherein at least one of the first communication interface and the second communication interface comprises a standard input/output interface configured to receive the additional previously presented instructions *[Borkar; the input/output ports of the communication agent communicate instructions of the system (section 2.1), which include the additional previously presented instructions]*.

16. Referring to claim 16, Borkar and Barat have taught the system of claim 1 wherein at least one of the first communication interface and the second communication interface comprises a multiplexer/demultiplexer *[Borkar; since multiplex communication is performed (6th paragraph of section 4.1.1), there is inherently a multiplexer/demultiplexer]*.

17. Referring to claim 18, Borkar has taught a method for a system with multiple processor nodes, the method comprising:

executing an application in at least one processing element *[computation agent; Fig. 1]* in a plurality of the processor nodes *[iWarp cells; Fig. 1] [section 2.1]*;

communicating using a first communication interface *[first input port/output port pair]* including a first array interface module *[first input port]* configured to interface to a first other member of the plurality of processor nodes *[section 2.1]*;

determining if a neighboring device is a member of the plurality of processor nodes *[Since communication depends upon the neighboring device, there is inherently a determination if the neighboring device is a member of the plurality of iWarp cells; section 2.2]*;

if the neighboring device is a member of the plurality of processor nodes, communicating to the neighboring device using a second communication interface including a second array interface module *[If the neighboring device is one of the iWarp cell, then communicate using the second input/output port pair; 2nd paragraph of section 2.2]*;

if the neighboring device is not a member of the plurality of processor nodes, communicating to the neighboring device using a standard input/output interface of the second communication interface *[If*

the neighboring device is not one of the iWarp cells, then communicate using a first port of the peripheral interface; 3rd paragraph of section 2.2].

Borkar has not taught providing an additional new instruction to a set of standard instructions for the processing element, using at least one software extensible device in the plurality of the processor nodes, wherein the new instructions can be programmed by software.

Barat has taught providing an additional new instruction to a set of standard instructions for a microprocessor, using at least one reconfigurable processing unit (RPU) in a processor node, wherein the new instructions can be programmed by *[section 1, "Introduction"]*.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the iWarp cells of Borkar to each comprise a software extensible device (i.e. an RPU) coupled to the computation unit of each iWarp cell thereby providing an additional new instruction to a set of standard instructions for the computation unit wherein the new instructions can be programmed by software as taught by Barat.

The suggestion/motivation for doing so would have been that processing is more specialized thereby accelerating execution and increasing performance *[section 1, "Introduction"]*.

18. Referring to claim 24, Borkar and Barat have taught the method of claim 18 further comprising compiling the application *[Borkar; It is inherent that in order to execute the application it must be compiled]*.

19. Referring to claim 25, Borkar and Barat have has taught the method of claim 18 further comprising loading the application into one of the plurality of the processor nodes *[Borkar; It is inherent that in order for an application to be executed in a processor node the application is loaded into the node]*.

20. Referring to claim 26, Borkar and Barat have taught the method of claim 18 further comprising configuring one of the processor nodes to select between an array interface module and a standard input/output interface based on a type of the neighboring device *[Borkar; communication depends on* whether the neighboring device is a peripheral or iWarp cell (section 2.2). Therefore, there is inherently a selection between the iWarp cell interface and the peripheral interface].

21. Referring to claim 31, Borkar and Barat have taught the system of claim 1 wherein each processor node further comprises:

a third communication interface [Borkar; third input port/output port pair] including a third array interface module configured to interface to a third other member of the plurality of processor nodes, and

a third standard input/output interface [Borkar; third input port/output port pair] configured to communicate with a third input/output device [Borkar; section 2.1], and

a fourth communication interface [Borkar; fourth input port/output port pair] including a fourth array interface module configured to interface to a fourth other member of the plurality of processor nodes, and

a fourth standard input/output interface [Borkar; fourth input port/output port pair] configured to communicate with a fourth input/output device [Borkar; section 2.1].

22. Referring to claim 32, Borkar and Barat have taught the system of claim 1 wherein the first communication interface is configured to communicate through the first array interface module if the first communication interface is coupled to the first other member of the plurality of processor nodes, and to communicate through the first standard input/output interface if the first communication interface is coupled to the first input/output device [Borkar; section 2.1].

23. Referring to claim 33, Borkar and Barat have taught the system of claim 1 wherein two or more of the plurality of processor nodes are configured in a one-dimensional array [Borkar; 5th paragraph of Introduction; section 3].

24. Referring to claim 34, Borkar and Barat have taught the system of claim 1 wherein three or more of the plurality of the processor nodes are configured in a non-rectangular configuration [Borkar; 5th paragraph of Introduction; section 3].

25. Referring to claim 35, Borkar and Barat have taught the system of claim 10 wherein the time division multiplexing provides a guaranteed bandwidth for a communication between the processor nodes [Borkar; 6th paragraph of section 4.1.1].

26. Referring to claim 36, Borkar and Barat have taught the system of claim 1 wherein the first communication interface is configured to guarantee a bandwidth for a communication between two of the plurality of processor nodes [Borkar; 6th paragraph of section 4.1.1].

27. Referring to claim 37, Borkar and Barat have taught the method of claim 18 further comprising:

determining if another neighboring device is a member of the plurality of the processor nodes [Borkar; Since communication depends upon the neighboring device, there is inherently a determination if the neighboring device is a member of the plurality of iWarp cells; section 2.2];

if the another neighboring device is a member of the plurality of processor nodes, communicating to the another neighboring device using a third communication interface including a third array interface module [Borkar; If the neighboring device is one of the iWarp cell, then communicate using the third input/output port pair; 2nd paragraph of section 2.2]; and

if the another neighboring device is not a member of the plurality of processing nodes, communicating to the neighboring device using a standard input/output interface of the third communication interface [Borkar; If the neighboring device is not one of the iWarp cells, then communicate using a second port of the peripheral interface; 3rd paragraph of section 2.2].

28. Referring to claim 38, Borkar and Barat have taught the method of claim 18 wherein the communicating using the first communication interface uses the first array interface module and uses time division multiplexing, the time division multiplexing providing a guaranteed bandwidth for a communication to the first other member of the plurality of processing nodes [Borkar; 6th paragraph of section 4.1.1].

29. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Borkar in view of Barat and further in view of the examiner's taking of official notice.

30. Referring to claim 3, Borkar and Barat have taught the system of claim 1, wherein a single processor node (iWarp) is on a chip *[Borkar; 1st paragraph of introduction]*.

Borkar and Barat have not explicitly taught that at least two of the processor nodes are on the same chip.

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to modify the system of Borkar and Barat such that at least two iWarp cells (i.e. processor nodes) are on the same chip.

The motivation for doing so would have been to reduce communication latency caused by off-chip signal transmission as would have been recognized by one of ordinary skill in the art.

Response to Arguments

31. Applicant's arguments filed 11/07/2007 have been fully considered but they are not persuasive.

32. Applicant argues the novelty/rejection of the claims, in substance that:

a. "First, there is no motivation to combine the RPU of Barat with the iWarp of Borkar" (page 10)

b. "Second, even if the RPU of Barat were combined with Borkar, the Examiner has not established an expectation of success in 'accelerating execution and increasing performance'" (page 11)

c. "Third, Barat teaches away from the combination" (page 11)

d. "There is no teaching or suggestion that in survey article [Barat] of using an RPU in a processor array or with multiple processors" (page 12)

e. "[N]either Borkar nor Barat teach 'a first standard input/output interface configured to communicate with a first input/output device ... and a second standard input/output interface configured to communicate with a second input/output device'" (page 15)

f. "[T]he missing element of 'determining if a neighboring device is a member of a plurality of processor nodes' is not inherent" (page 18)

33. These arguments are not found persuasive for the following reasons:

34. Regarding point a, the examiner notes that Barat specifically directed at combining a microprocessor with reconfigurable logic (i.e. a software extensible device). Barat states that a benefit of this combination is that the reconfigurable processor combination would "accelerate the execution of the

applications it was designed for." [section 1; 1st and 2nd paragraphs] Therefore, this is a motivation to combine the RPU of Barat with the iWarp of Borkar.

35. Regarding point b, although Barat states that there is not always an improvement from adding an RPU to a processor, Barat as a whole is directed at coupling processors with an RPU. The cases where an improvement is not obtained are the exceptions, while the general case is that where an improvement is obtained. Therefore, there it would have been reasonably expected that combining an RPU as taught by Barat with the processing circuitry of an iWarp cell would result in accelerated execution.

36. Regarding point c, the examiner disagrees with applicant's assertion that "Barat teaches away from the combination" of Borkar and Barat. While Barat indicates that in certain situations combining an RPU with a VLIW processor would result in a performance loss, Barat also notes a technique for coupling reconfigurable logic with a VLIW that would not result in a performance loss [section 2.5; 5th paragraph]. Therefore, Barat has not taught away from the combination of Borkar and Barat.

37. Regarding point d, the examiner notes that the Barat survey is directed at coupling reconfigurable logic at the processing unit level. Barat is not concerned with and is not relied upon for teaching the specific application (e.g. processing array) of the reconfigurable instruction set processor. Whether Barat suggests using an RPU in a processing unit wherein the processing unit is part of an array of processing units is irrelevant since Borkar is relied upon as teaching the processing array.

38. Regarding point e, the examiner notes that the applicant appears to be reading the claim language too narrowly. The claims recite processing nodes that comprise "a first standard input/output interface configured to communicate with a first and input/output device" and "a second standard input/output interface configured to communicate with a second and input/output device". Borkar has taught iWarp cells that comprise 4 input/output ports (i.e. standard input/output interfaces) configured to communicate with other iWarp cells (i.e. input/output devices) [section 2.1]. Since the iWarp cells are devices that input and output data, they are input/output devices. The applicant appears to be reading the above-cited limitations such that the standard input/output interfaces communicate with a specific type of input/output device. However, the claim language does not require such a reading. If the applicant

intends for the claimed input/output device to be of a specific type, then the applicant such amend the claim to indicate the specific type of device.

39. Regarding point f, the examiner notes that a given iWarp cell has ability to communicate with neighboring devices that include iWarp cells and other peripheral devices. Depending on which neighboring device the iWarp cell wants to communicate with, the cell communicates using either the communication agent (in the case that the neighboring device is an iWarp cell) or the local memory peripheral interface (in the case that the neighboring device is not an iWarp cell) [section 2.2]. Therefore, the iWarp cell must make a determination whether the neighboring device that it wants to communicate with is a member of the plurality of processing nodes (i.e. iWarp cells).

Conclusion

40. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin P. Geib whose telephone number is (571) 272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Benjamin P Geib
Examiner
Art Unit 2181

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01/31/2008